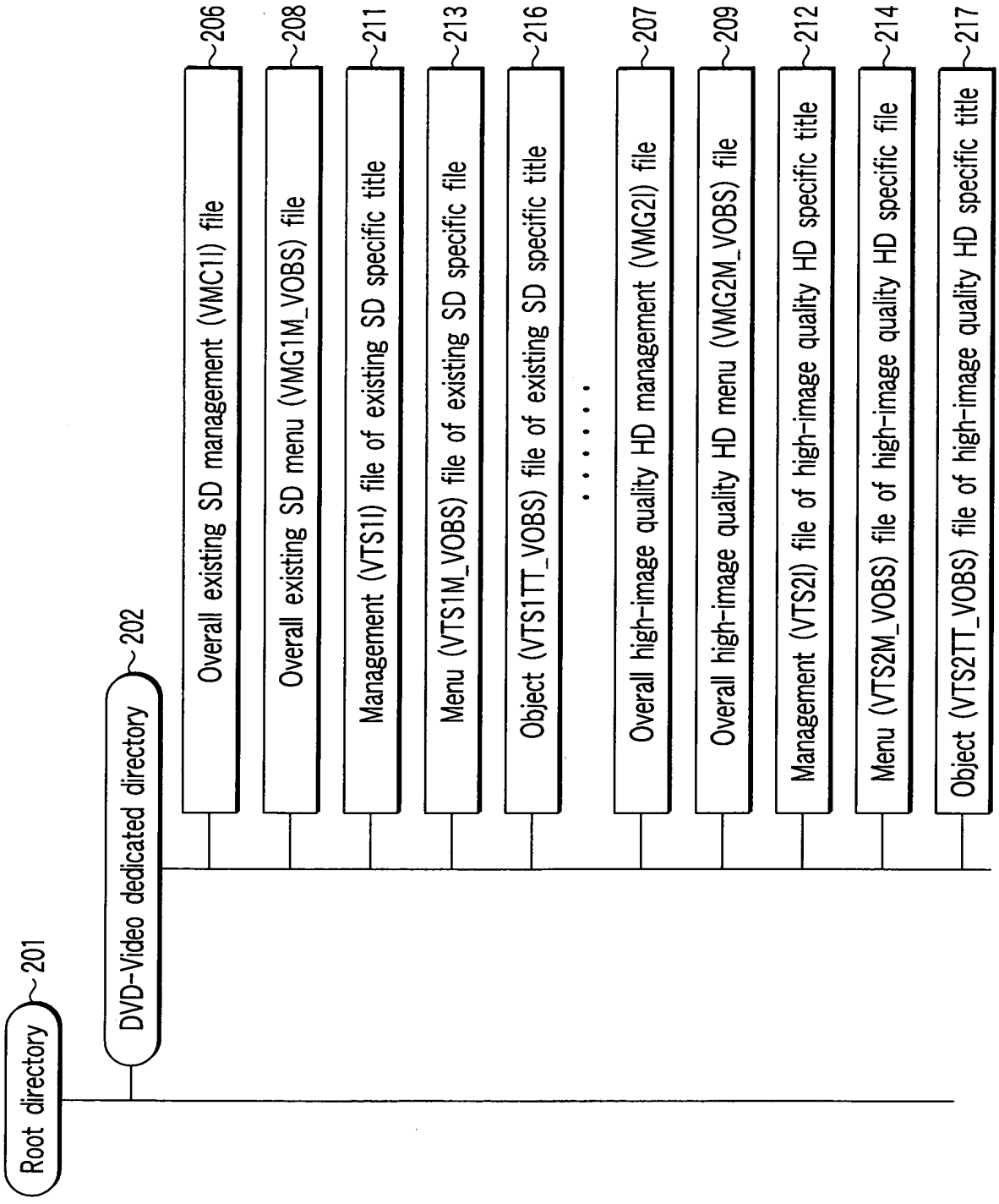

Root directory
201
DVD-Video dedicated directory
202
Overall existing SD management (VMC1I) file
206
Overall existing SD menu (VMG1M_VOBS) file
208
Management (VTS1I) file of existing SD specific title
211
Menu (VTS1M_VOBS) file of existing SD specific file
213
Object (VTS1TT_VOBS) file of existing SD specific title
216
Overall high-image quality HD management (VMG2I) file
207
Overall high-image quality HD menu (VMG2M_VOBS) file
209
Management (VTS2I) file of high-image quality HD specific title
212
Menu (VTS2M_VOBS) file of high-image quality HD specific file
214
Object (VTS2TT_VOBS) file of high-image quality HD specific title
217

FIG. 1

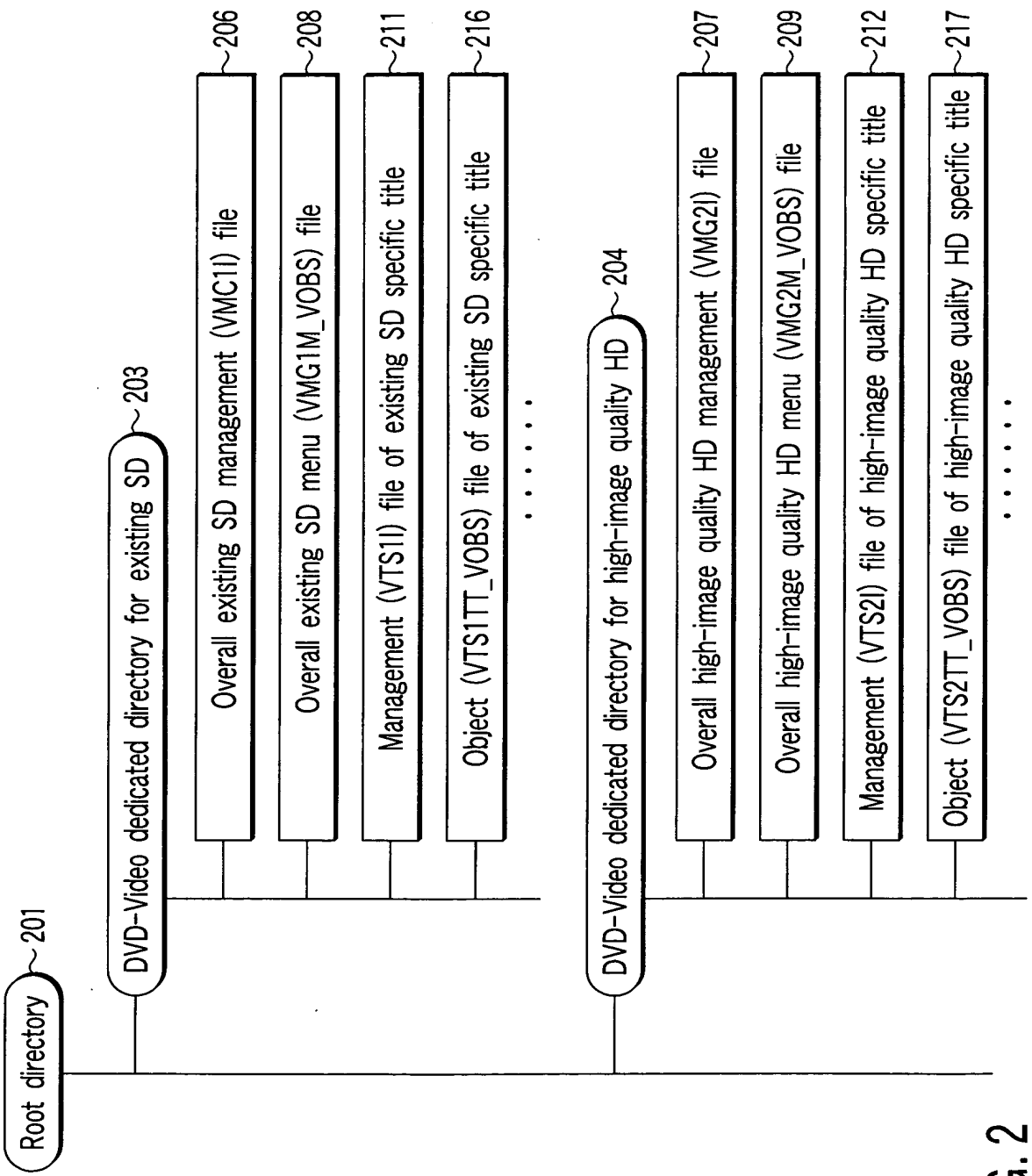

Root directory
201
DVD-Video dedicated directory for existing SD
203
Overall existing SD management (VMC1I) file
206
Overall existing SD menu (VMG1M_VOBS) file
208
Management (VTS1I) file of existing SD specific title
211
Object (VTS1TT_VOBS) file of existing SD specific title
216
DVD-Video dedicated directory for high-image quality HD
204
Overall high-image quality HD management (VMG2I) file
207
Overall high-image quality HD menu (VMG2M_VOBS) file
209
Management (VTS2I) file of high-image quality HD specific title
212
Object (VTS2TT_VOBS) file of high-image quality HD specific title
217

FIG. 2

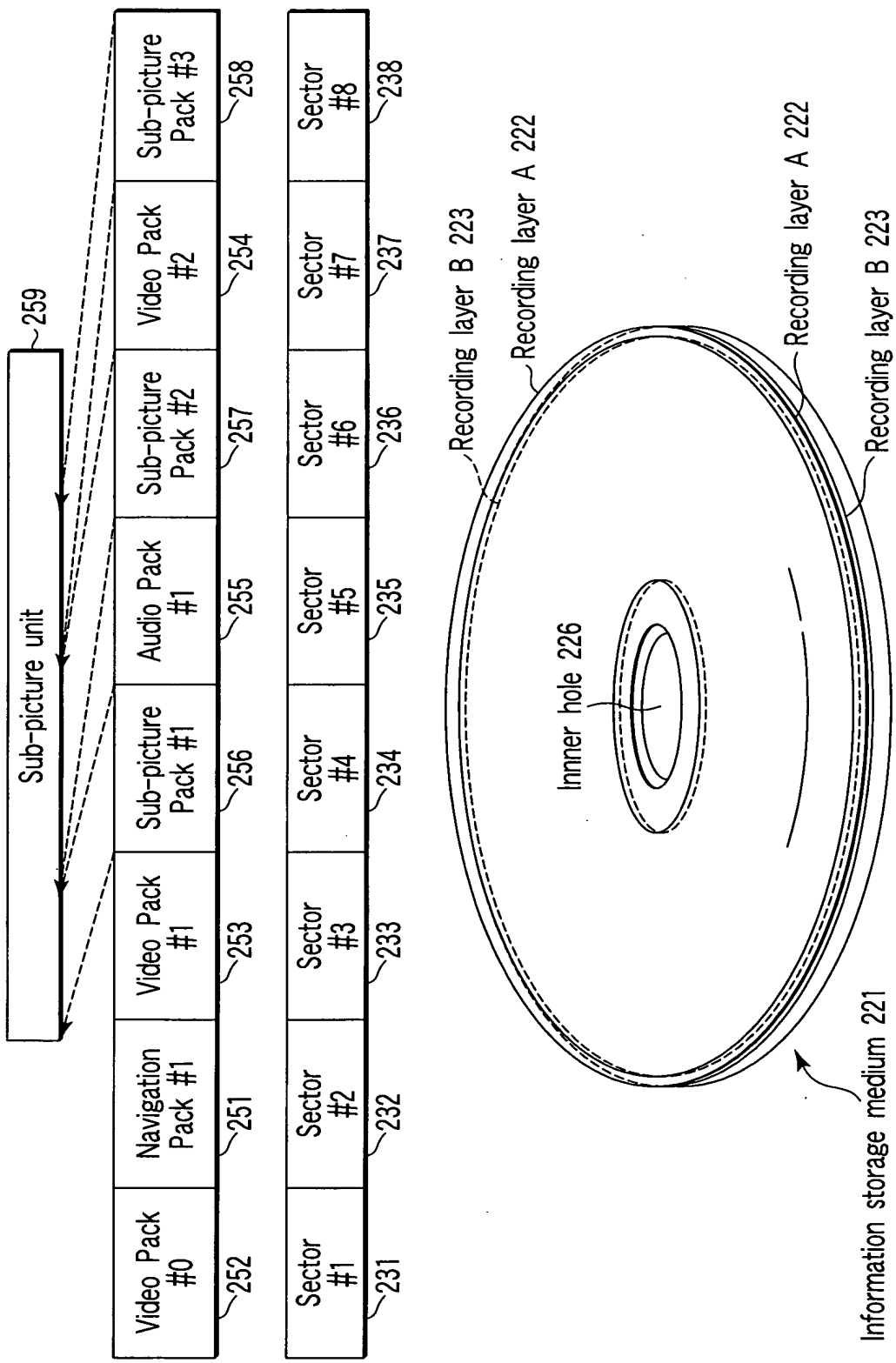

Sub-picture unit
259
Video Pack #0
252
Navigation Pack #1
251
Video Pack #1
253
Sub-picture Pack #1
256
Audio Pack #1
255
Sub-picture Pack #2
257
Video Pack #2
254
Sub-picture Pack #3
258
Sector #1
231
Sector #2
232
Sector #3
233
Sector #4
234
Sector #5
235
Sector #6
236
Sector #7
237
Sector #8
238
Recording layer B 223
Recording layer A 222
Inner hole 226
Recording layer A 222
Recording layer B 223
Information storage medium 221

FIG. 3

Compression rule explanatory view (1)

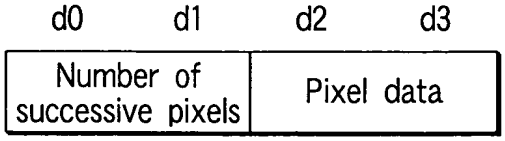


FIG. 4A

Compression rule explanatory view (2)

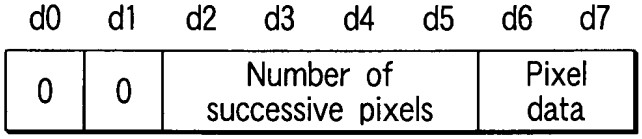


FIG. 4B

Compression rule explanatory view (3)

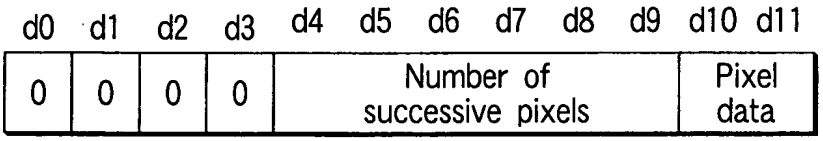


FIG. 4C

Compression rule explanatory view (4)

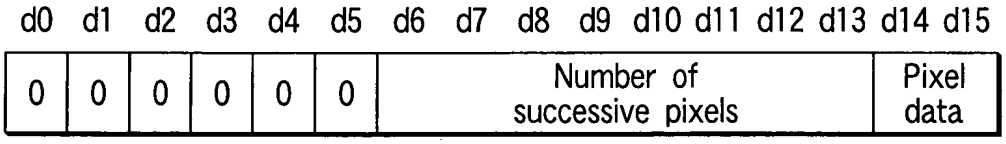


FIG. 4D

Compression rule (5)

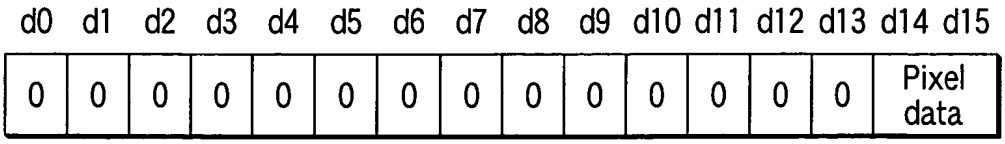


FIG. 4E

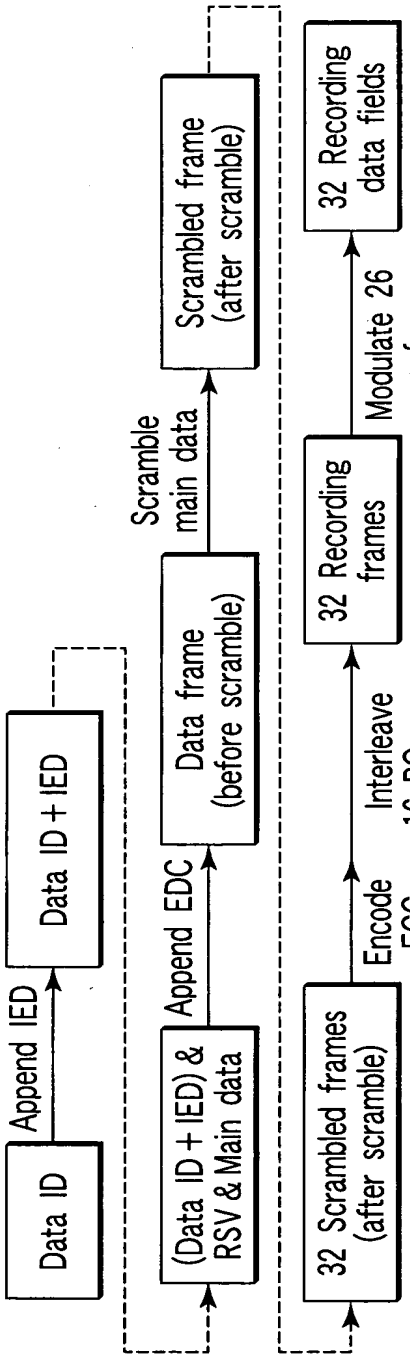

Data ID
Append IED
Data ID + IED
(Data ID + IED) & RSV & Main data
Append EDC
Data frame (before scramble)
Scramble main data
Scrambled frame (after scramble)
32 Scrambled frames (after scramble)
Encode ECC
Interleave 16 PO rows
32 Recording frames
Modulate 26 sync frames
32 Recording data fields

FIG. 5

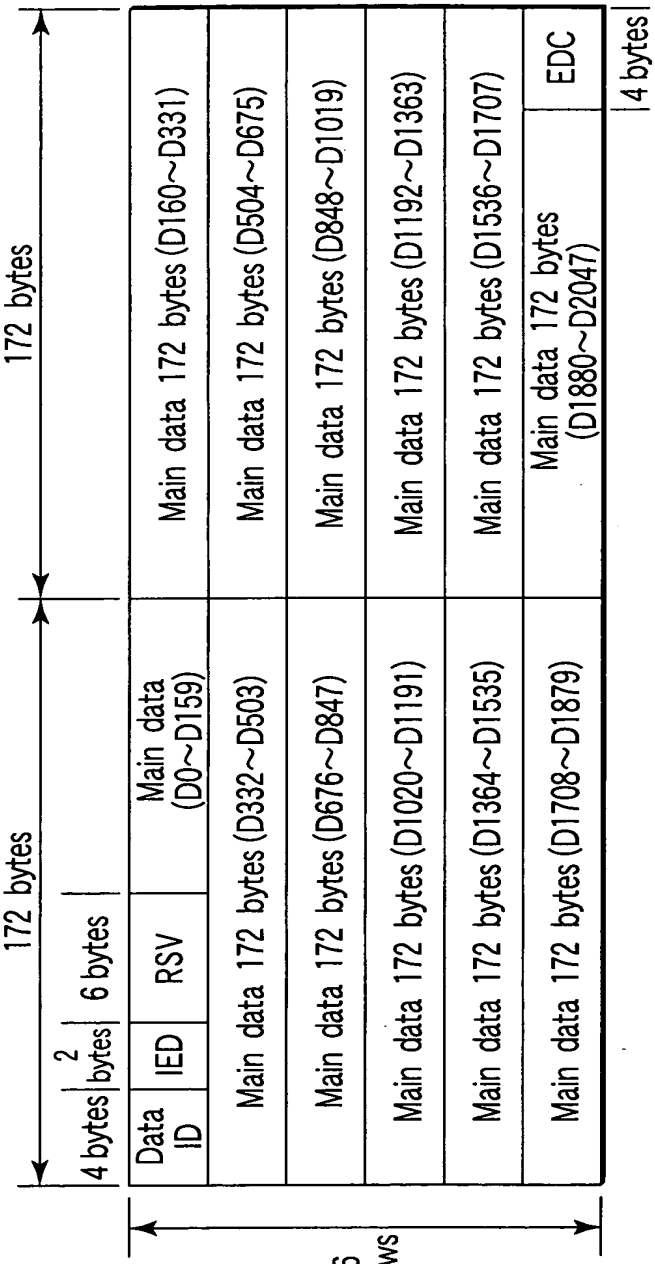

172 bytes
172 bytes
4 bytes
2 bytes
6 bytes
Data ID
IED
RSV
Main data (D0~D159)
Main data 172 bytes (D160~D331)
Main data 172 bytes (D332~D503)
Main data 172 bytes (D504~D675)
Main data 172 bytes (D676~D847)
Main data 172 bytes (D848~D1019)
Main data 172 bytes (D1020~D1191)
Main data 172 bytes (D1192~D1363)
Main data 172 bytes (D1364~D1535)
Main data 172 bytes (D1536~D1707)
Main data 172 bytes (D1708~D1879)
Main data 172 bytes (D1880~D2047)
EDC
4 bytes
6 rows

FIG. 6

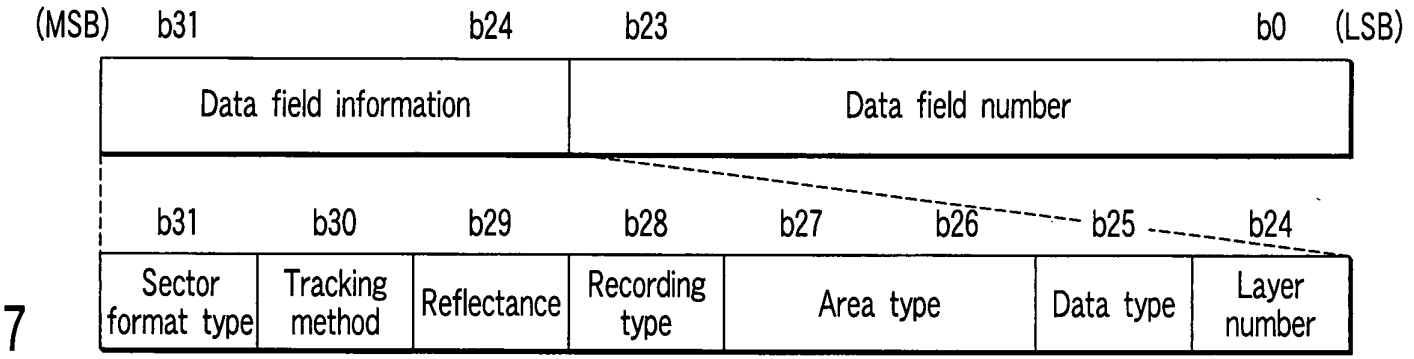


FIG. 7

Area	Contents
Embossed data zone	Sector number
Defect management area	Sector number
Disc identification zone	Sector number
Used block of data area	LSN + 031000h
Unused block of data area	State 1 : first 3 bits = 0, incremented number follows State 2 : from 00 0000h to 00 00Hh State 3 : unrecorded

FIG. 8

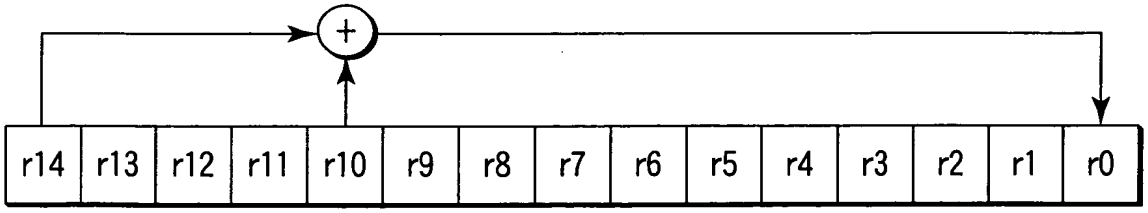
Area		Contents
Embossed data zone		Reserved
Rewritable data zone	Lead-in area Lead-out area	Reserved
	Data area	0b : general data 1b : real-time data

FIG. 9

Initial preset number	Initial preset value	Initial preset number	Initial preset value
0h	0001h	8h	0010h
1h	5500h	9h	5000h
2h	0002h	0Ah	0020h
3h	2A00h	0Bh	2001h
4h	0004h	0Ch	0040h
5h	5400h	0Dh	4002h
6h	0008h	0Eh	0080h
7h	2800h	0Fh	0005h

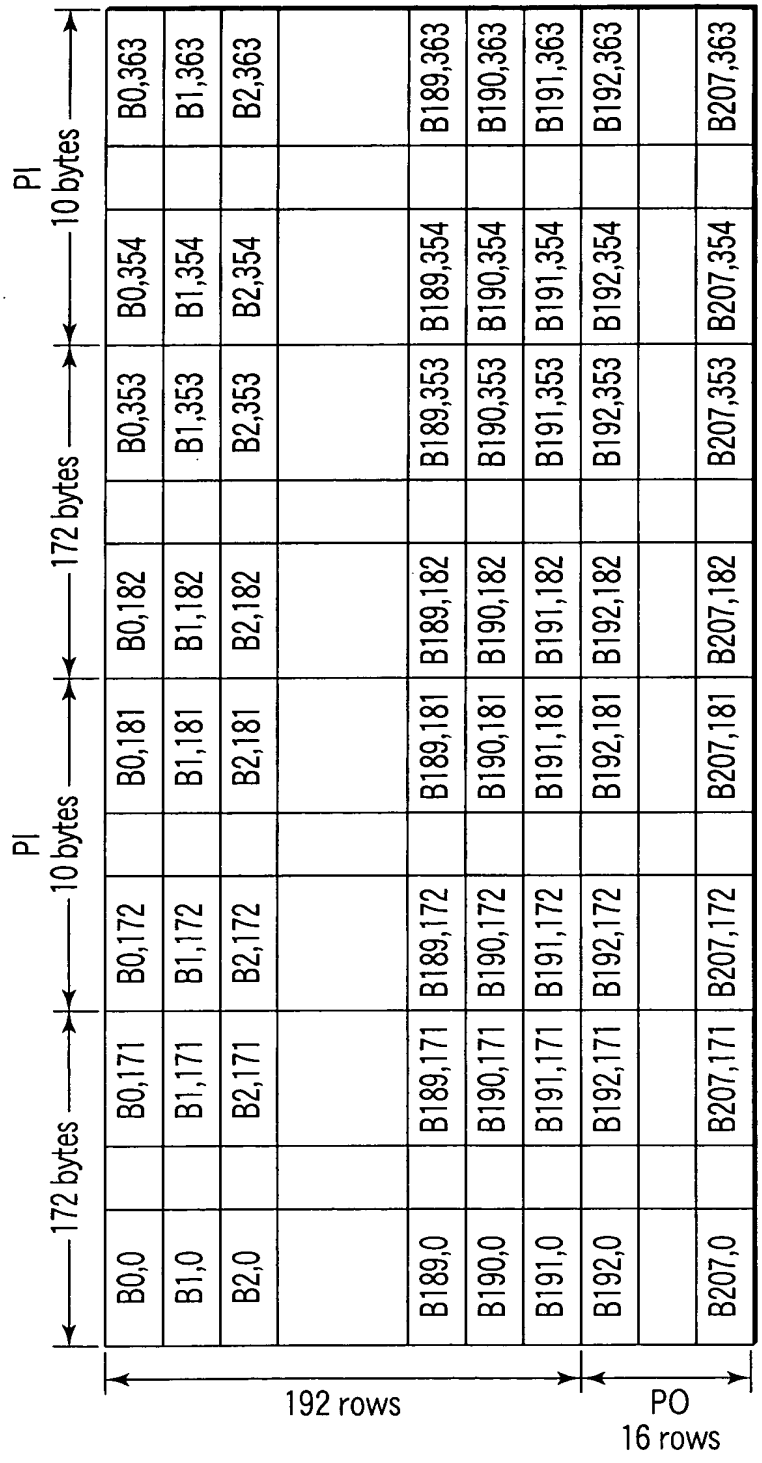
Initial value of shift register

FIG. 10A



Feedback shift register

FIG. 10B



(ECC block structure (D,E))

FIG. 11

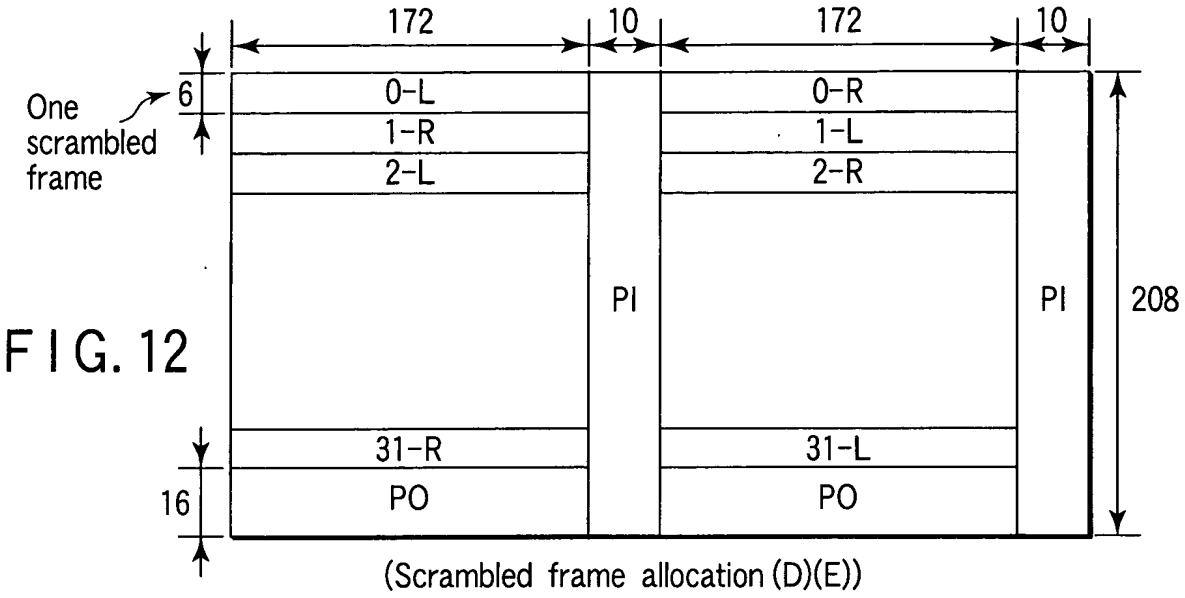


FIG. 12

(Scrambled frame allocation (D)(E))

Even Recorded data field:

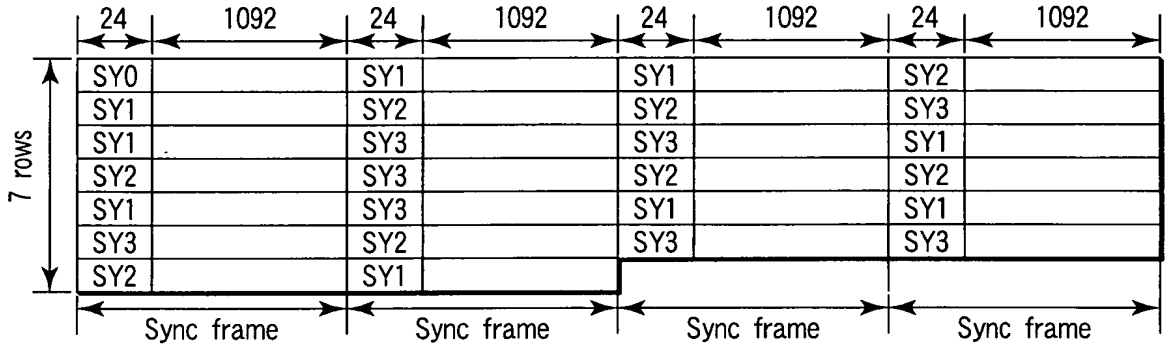


FIG. 14A

Odd Recorded data field:

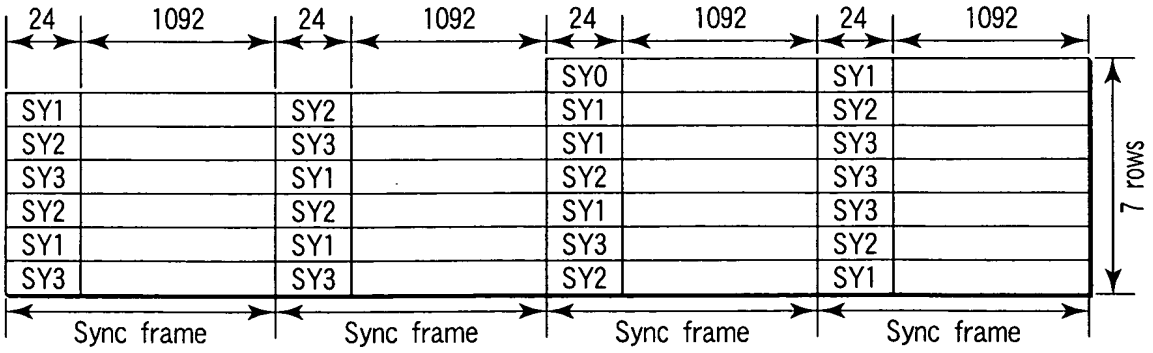


FIG. 14B

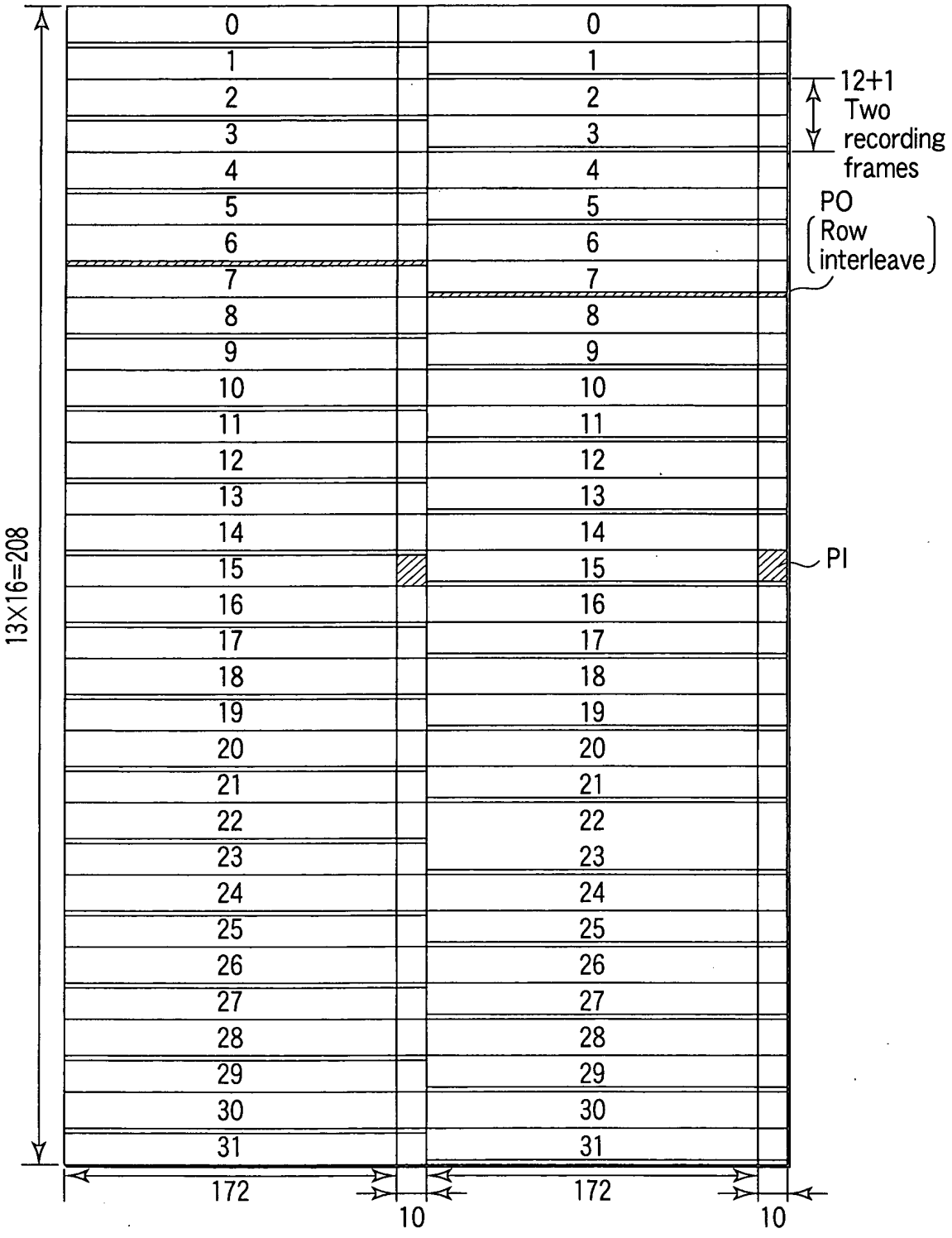

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
12+1
Two
recording
frames
PO
Row
interleave
PI
13X16=208
172
10
172
10

FIG. 13

State0

		(MSB) Primary SYNC codes (LSB)					(MSB) Secondary SYNC codes (LSB)			
SY0	=	000010	101000	000000	001001	/	000010	001000	000000	001001
SY1	=	100001	001000	000000	001001	/	100010	101000	000000	001001
SY2	=	100100	001000	000000	001001	/	101000	101000	000000	001001
SY3	=	101000	001000	000000	001001	/	101010	001000	000000	001001

State1

		(MSB) Primary SYNC codes (LSB)					(MSB) Secondary SYNC codes (LSB)			
SY0	=	000100	101000	000000	001001	/	000100	001000	000000	001001
SY1	=	001001	001000	000000	001001	/	001010	101000	000000	001001
SY2	=	010000	101000	000000	001001	/	010000	001000	000000	001001
SY3	=	010100	001000	000000	001001	/	010101	001000	000000	001001

FIG. 15

Comparison of combination patterns (column direction) of successive sync codes (1)
— upon moving between sectors —

Latest sync frame number	00	01	02	03	04	05	06	07	08	09	10	11	12
Sync code number two codes before	2	1	0	1	1	2	1	2	2	3	1	3	3
Sync code number one code before	1	0	1	1	2	1	2	2	3	1	3	3	1
Latest sync code number	0	1	1	2	1	2	2	3	1	3	3	1	2
Number of code changes between neighboring patterns	3	2	2	2	3	2	2	2	3	2	2	2	3
Number of code changes shifted by one frame	2	2	2	1	1	2	3	2	2	2	3	3	2

Latest sync frame number	13	14	15	16	17	18	19	20	21	22	23	24	25
Sync code number two codes before	1	2	3	2	2	1	3	1	1	3	2	3	3
Sync code number one code before	2	3	2	2	1	3	1	1	3	2	3	3	2
Latest sync code number	3	2	2	1	3	1	1	3	2	3	3	2	1
Number of code changes between neighboring patterns	3	2	2	2	3	2	2	2	3	2	2	2	3
Number of code changes shifted by one frame	2	2	3	2	2	2	3	2	2	2	3	3	2

FIG. 16

Comparison of combination patterns (column direction) of successive sync codes (2)
— upon extending across guard area —

Latest sync frame number	00	01	02	03	04	05	06	07	08	09	10	11	12
Sync code number two codes before	1	1	0	1	1	2	1	2	2	3	1	3	3
Sync code number one code before	1	0	1	1	2	1	2	2	3	1	3	3	1
Latest sync code number	0	1	1	2	1	2	2	3	1	3	3	1	2
Number of code changes between neighboring patterns	2	2	2	2	3	2	2	2	3	2	2	2	3
Number of code changes shifted by one frame	2	2	2	1	1	2	3	2	2	2	3	3	2

Latest sync frame number	13	14	15	16	17	18	19	20	21	22	23	24	25	PA
Sync code number two codes before	1	2	3	2	2	1	3	1	1	3	2	3	3	2
Sync code number one code before	2	3	2	2	1	3	1	1	3	2	3	3	2	1
Latest sync code number	3	2	2	1	3	1	1	3	2	3	3	2	1	1
Number of code changes between neighboring patterns	3	2	2	2	3	2	2	2	3	2	2	2	2	2
Number of code changes shifted by one frame	2	2	3	2	2	2	3	2	2	2	3	3	3	2

FIG. 17

Relationship with abnormal phenomenon upon detection of unexpected combination pattern of sync codes

Abnormal phenomenon contents→	Frame shift		Detection error		Tracking error
Detected pattern contents ↓	Case 1	Case 2	Case 3	Case 4	Case 5
Different by only one position from expected pattern	×	○	○	×	—
Match with pattern shifted from expected pattern by ±1 sync frame	○	○	×	×	× (△)
(1, 1, 2), (1, 2, 1), (1, 2, 2) or (2, 1, 2)	—	○	—	—	—
Continuity in data ID	(○)	(○)	○	○	×
Continuity of wobble addresses	(○)	(○)	○	○	×

FIG. 18

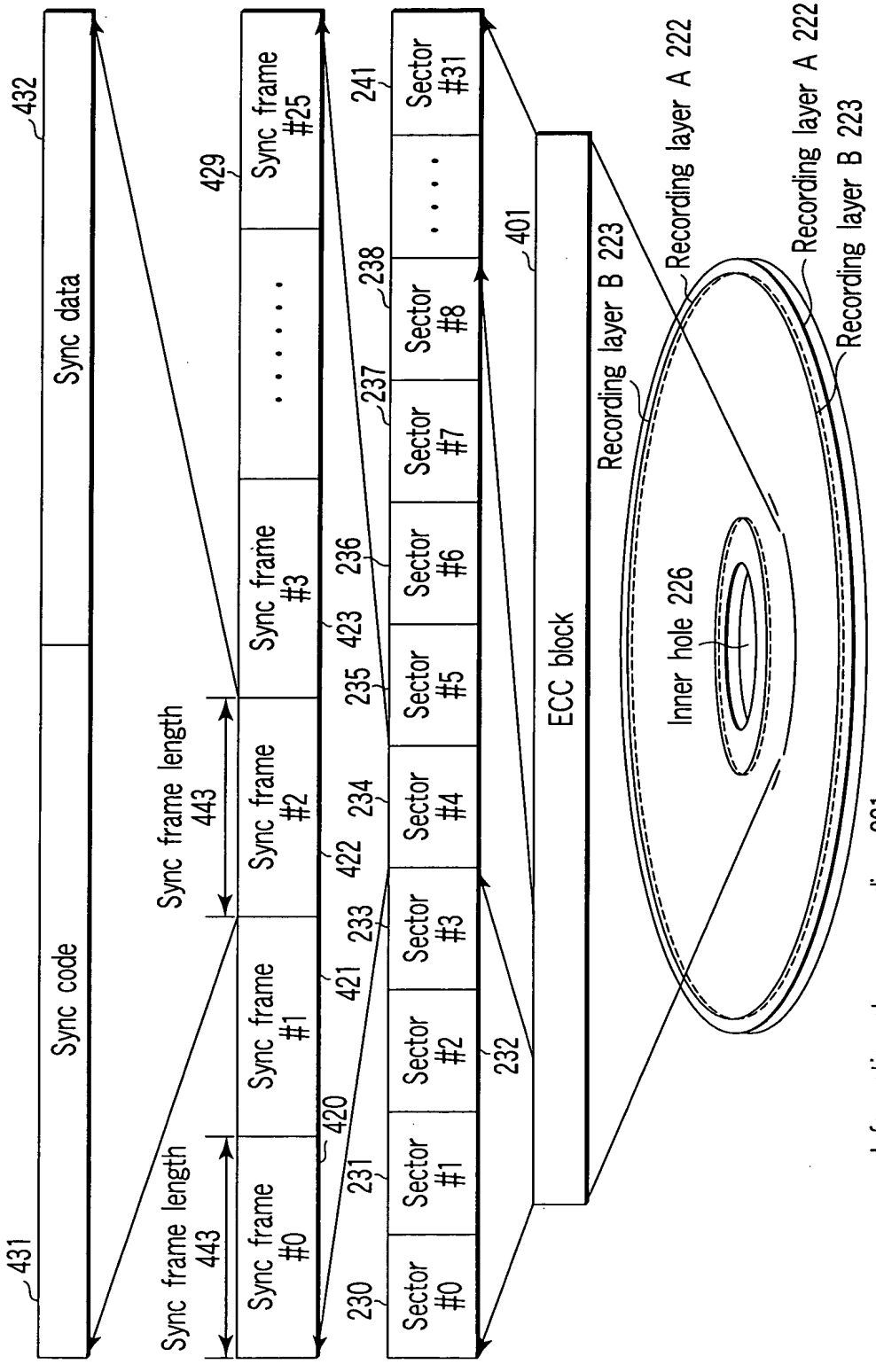

431
Sync code
432
Sync data
Sync frame length
443
Sync frame #0
Sync frame #1
Sync frame #2
Sync frame #3
429
Sync frame #25
420
421
422
423
Sector #0
Sector #1
Sector #2
Sector #3
Sector #4
Sector #5
Sector #6
Sector #7
Sector #8
Sector #31
230
231
232
233
234
235
236
237
238
241
401
ECC block
Recording layer B 223
Recording layer A 222
Inner hole 226
Recording layer A 222
Recording layer B 223
Information storage medium 221

FIG. 19

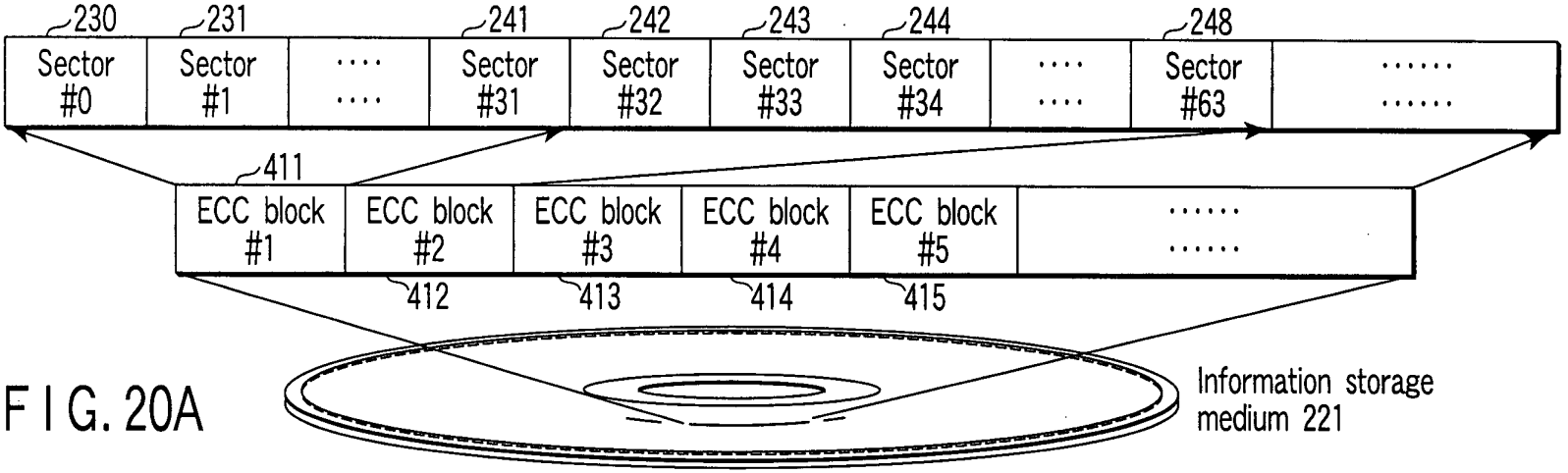


FIG. 20A

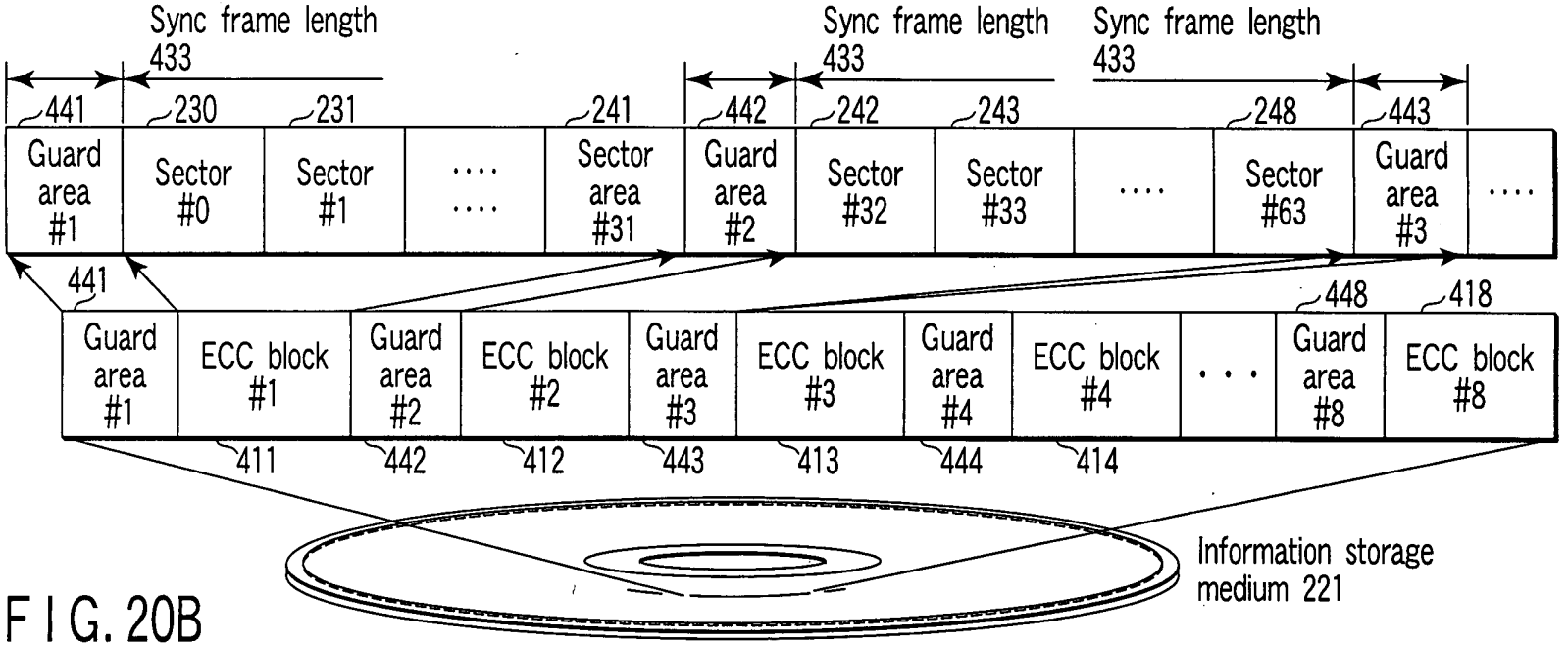


FIG. 20B

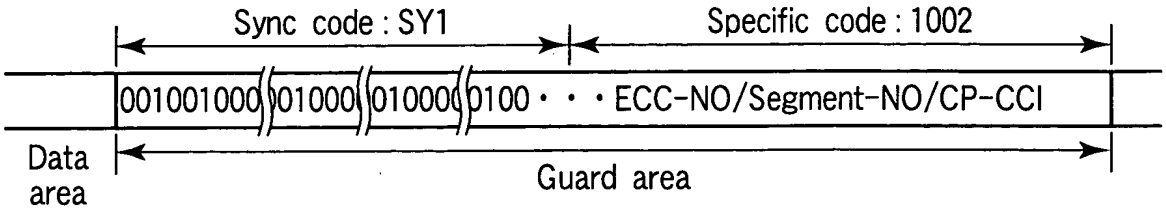


FIG. 21

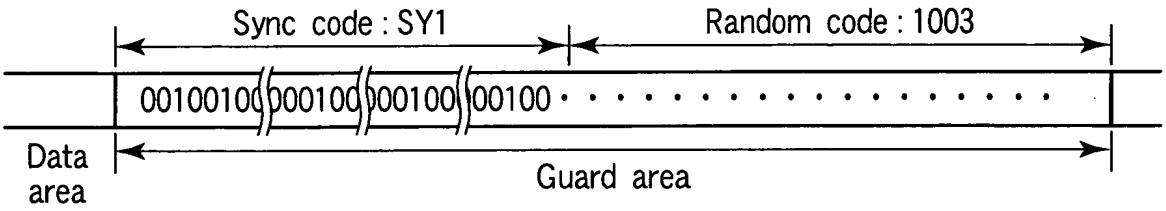


FIG. 22

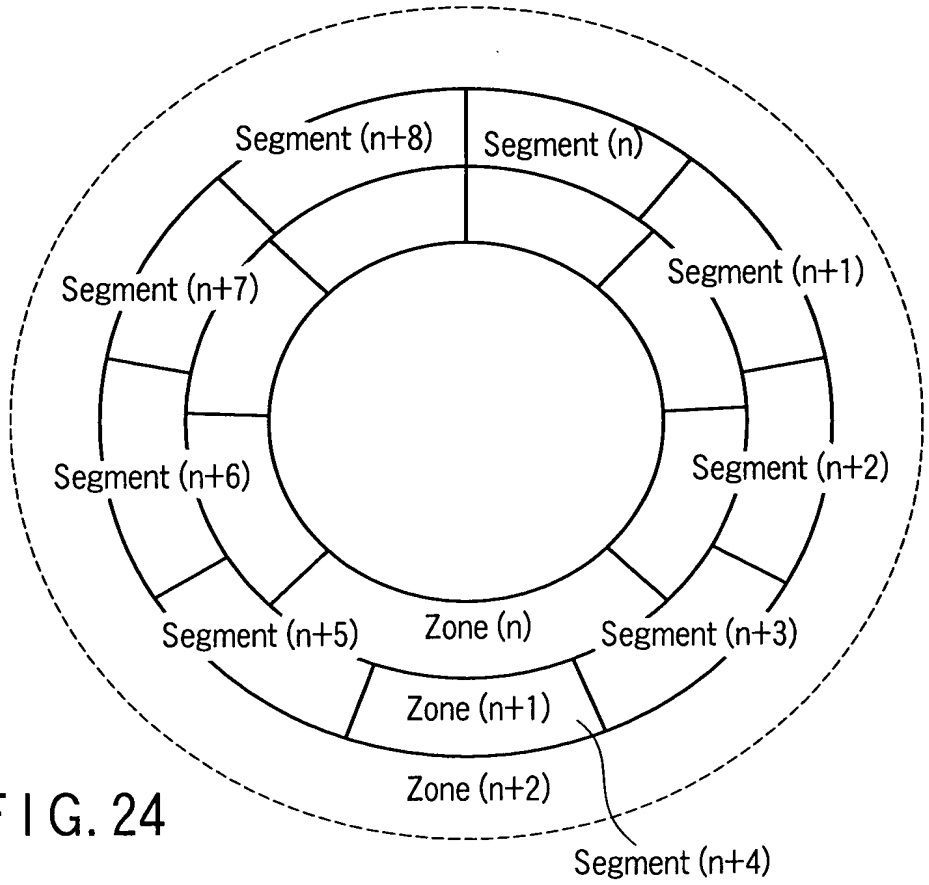


FIG. 24

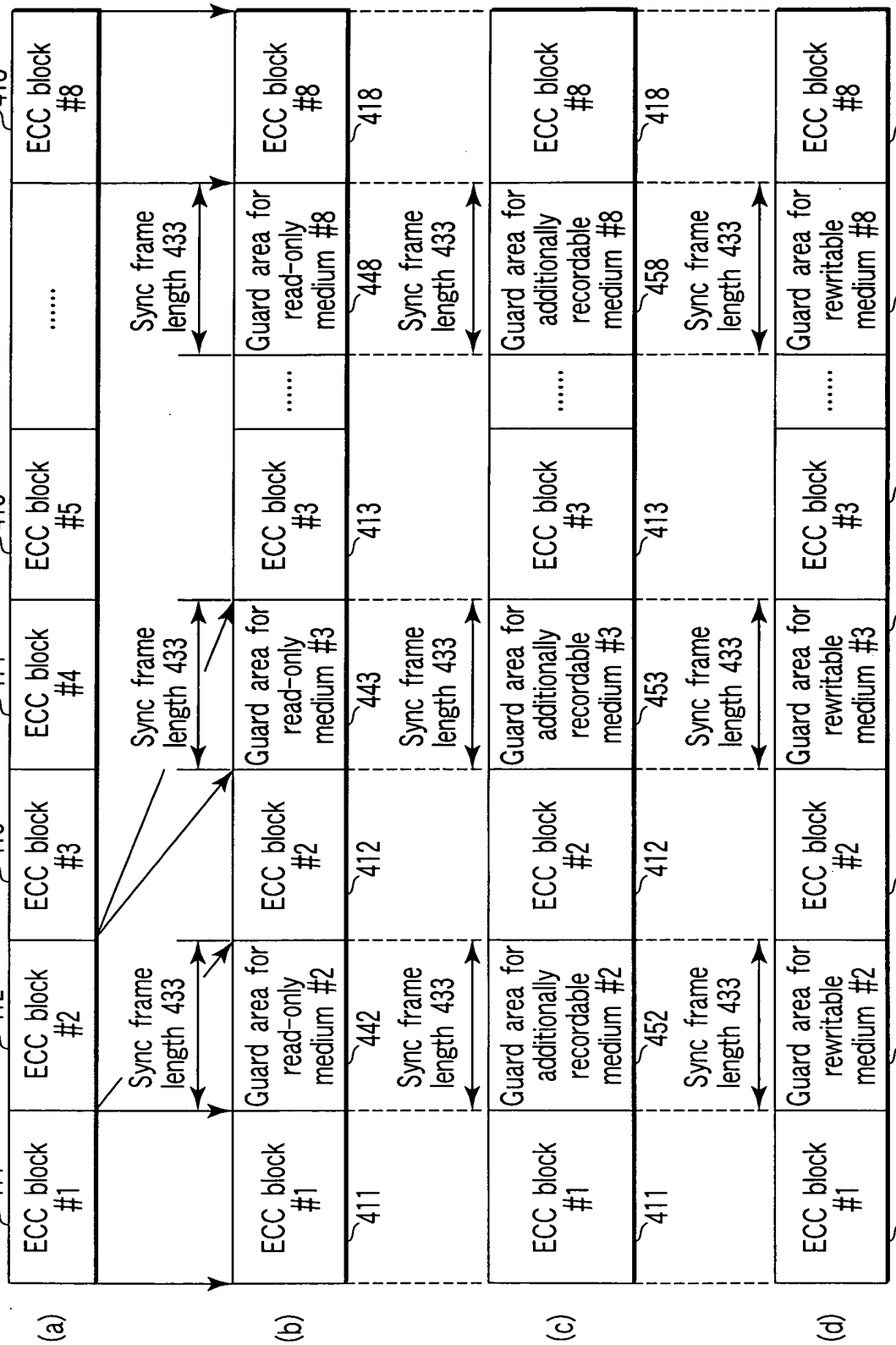
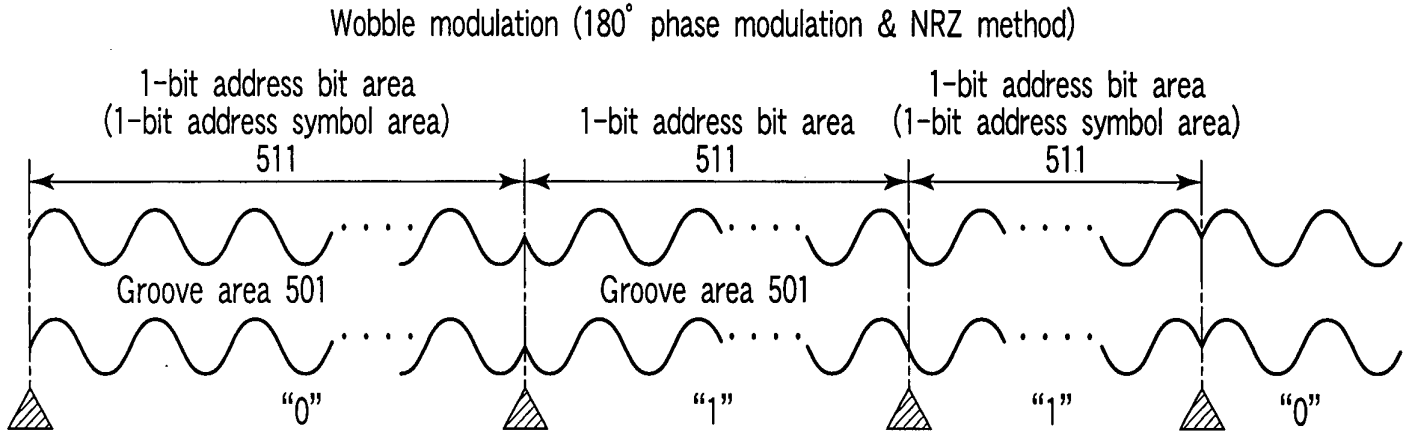

(a)
(b)
(c)
(d)
411
412
413
414
415
418
ECC block #1
ECC block #2
ECC block #3
ECC block #4
ECC block #5
.....
ECC block #8
Sync frame length 433
Guard area for read-only medium #2
Guard area for read-only medium #3
Guard area for read-only medium #8
Guard area for additionally recordable medium #2
Guard area for additionally recordable medium #3
Guard area for additionally recordable medium #8
Guard area for rewritable medium #2
Guard area for rewritable medium #3
Guard area for rewritable medium #8
442
443
448
452
453
458
462
463
468

FIG. 23



☆1-address bit area 511 (expressed by 8 or 12 wobbles)
☆ Frequency, amplitude, and phase of wobbles in 1-address bit area 511 = constant throughout area
☆ Boundary of 1-address bit area 511 (180° or 0° phase shift)

FIG. 25

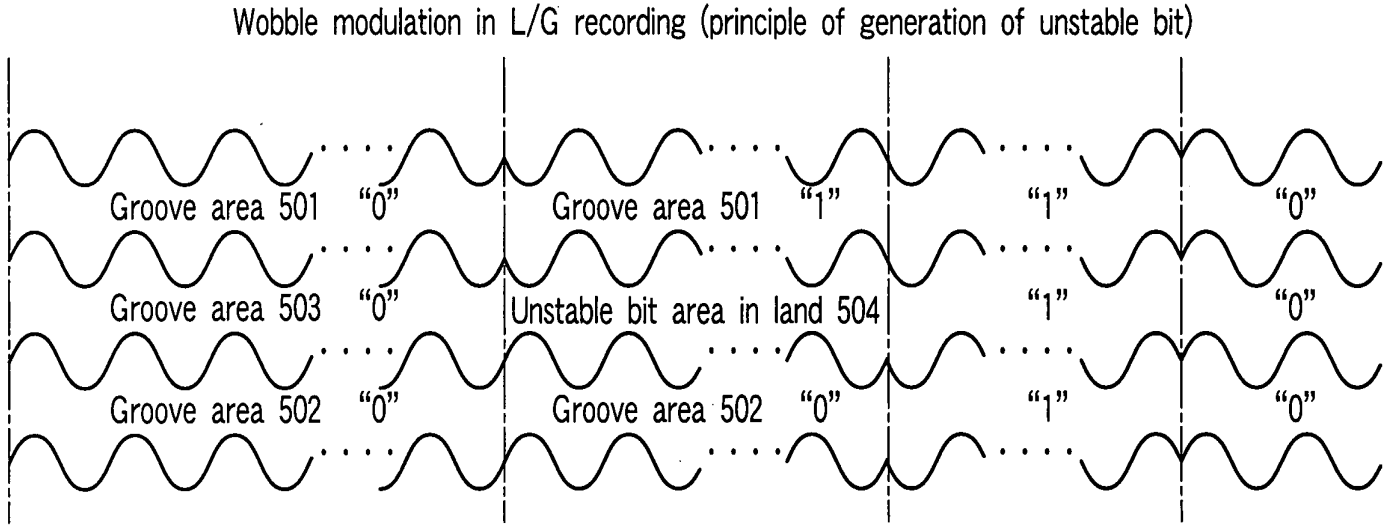


FIG. 26

Gray code example

Decimal value	Conventional binary notation	Gray code notation
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

FIG. 27

Special track code (present invention)

Decimal value	Conventional binary notation	Special track code	Decimal value	Conventional binary notation	Special track code
0	00000	00 ··· 00000	1	00001	10 ··· 00000
2	00010	00 ··· 00001	3	00011	10 ··· 00001
4	00100	00 ··· 00011	5	00101	10 ··· 00011
6	00110	00 ··· 00010	7	00111	10 ··· 00010
8	01000	00 ··· 00110	9	01001	10 ··· 00110
10	01010	00 ··· 00111	11	01011	10 ··· 00111
12	01100	00 ··· 00101	13	01101	10 ··· 00101
14	01110	00 ··· 00100	15	01111	10 ··· 00100
16	10000	00 ··· 01100	17	10001	10 ··· 01100
18	10010	00 ··· 01101	19	10011	10 ··· 01101
20	10100	00 ··· 01111	21	10101	10 ··· 01111
22	10110	00 ··· 01110	23	10111	10 ··· 01110
24	11000	00 ··· 01010	25	11001	10 ··· 01010
26	11010	00 ··· 01011	27	11011	10 ··· 01011
28	11100	00 ··· 01001	29	11101	10 ··· 01001
30	11110	00 ··· 01000	31	11111	10 ··· 01000

Note] only most significant bits are different, and remaining lower bits match in "2n" (n : integer value) and "2n+1"

FIG. 28

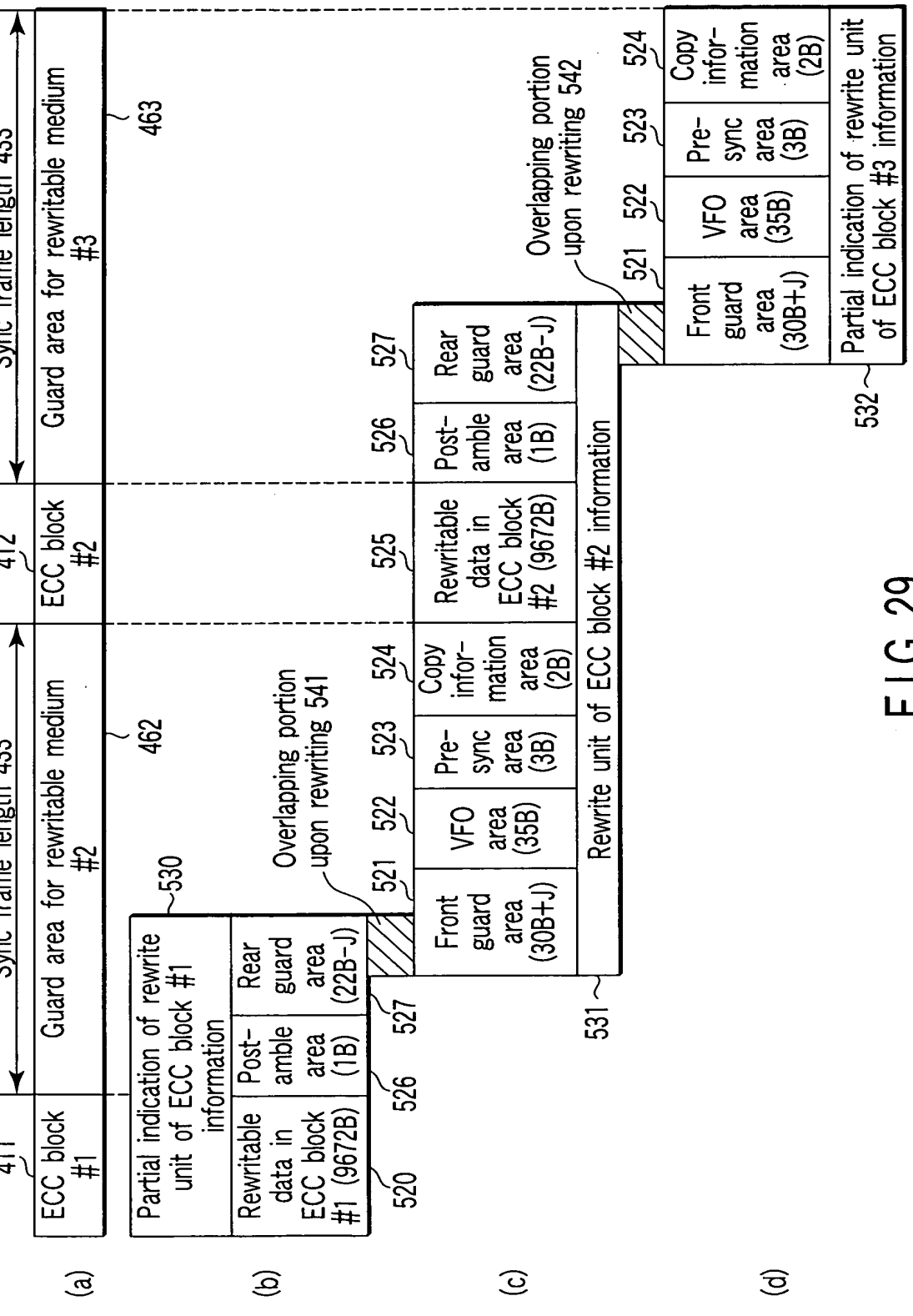

(a)
(b)
(c)
(d)
411
ECC block #1
Sync frame length 433
Guard area for rewritable medium #2
462
412
ECC block #2
Guard area for rewritable medium #3
463
530
Partial indication of rewrite unit of ECC block #1 information
Rewritable data in ECC block #1 (9672B)
520
Post-amble area (1B)
526
Rear guard area (22B-J)
527
Overlapping portion upon rewriting 541
521
Front guard area (30B+J)
522
VFO area (35B)
523
Pre-sync area (3B)
524
Copy infor-mation area (2B)
525
Rewritable data in ECC block #2 (9672B)
526
Post-amble area (1B)
527
Rear guard area (22B-J)
531
Rewrite unit of ECC block #2 information
Overlapping portion upon rewriting 542
521
Front guard area (30B+J)
522
VFO area (35B)
523
Pre-sync area (3B)
524
Copy infor-mation area (2B)
532
Partial indication of rewrite unit of ECC block #3 information

FIG. 29

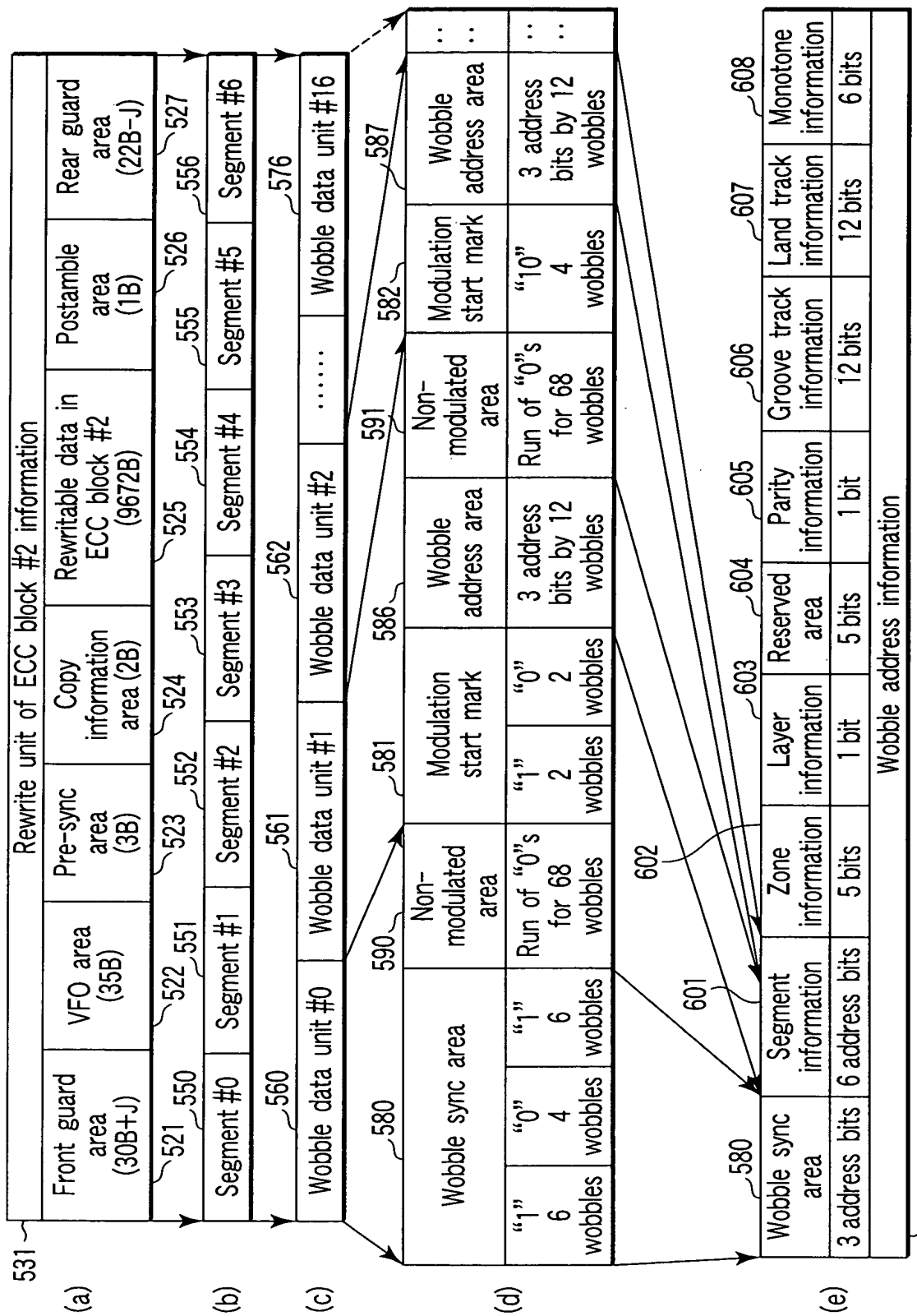

Rewrite unit of ECC block #2 information
Front guard area (30B+J)
VFO area (35B)
Pre-sync area (3B)
Copy information area (2B)
Rewritable data in ECC block #2 (9672B)
Postamble area (1B)
Rear guard area (22B-J)
Segment #0
Segment #1
Segment #2
Segment #3
Segment #4
Segment #5
Segment #6
Wobble data unit #0
Wobble data unit #1
Wobble data unit #2
Wobble data unit #16
Wobble sync area
Non-modulated area
Modulation start mark
Wobble address area
3 address bits by 12 wobbles
Run of "0"s for 68 wobbles
"1" 2 wobbles
"0" 2 wobbles
"1" 6 wobbles
"0" 4 wobbles
Segment information
Zone information
Layer information
Reserved area
Parity information
Groove track information
Land track information
Monotone information
6 address bits
5 bits
1 bit
12 bits
6 bits
Wobble address information
(a)
(b)
(c)
(d)
(e)
531
521
522
523
524
525
526
527
550
551
552
553
554
555
556
560
561
562
576
580
581
582
586
587
590
591
601
602
603
604
605
606
607
608
610

FIG. 30

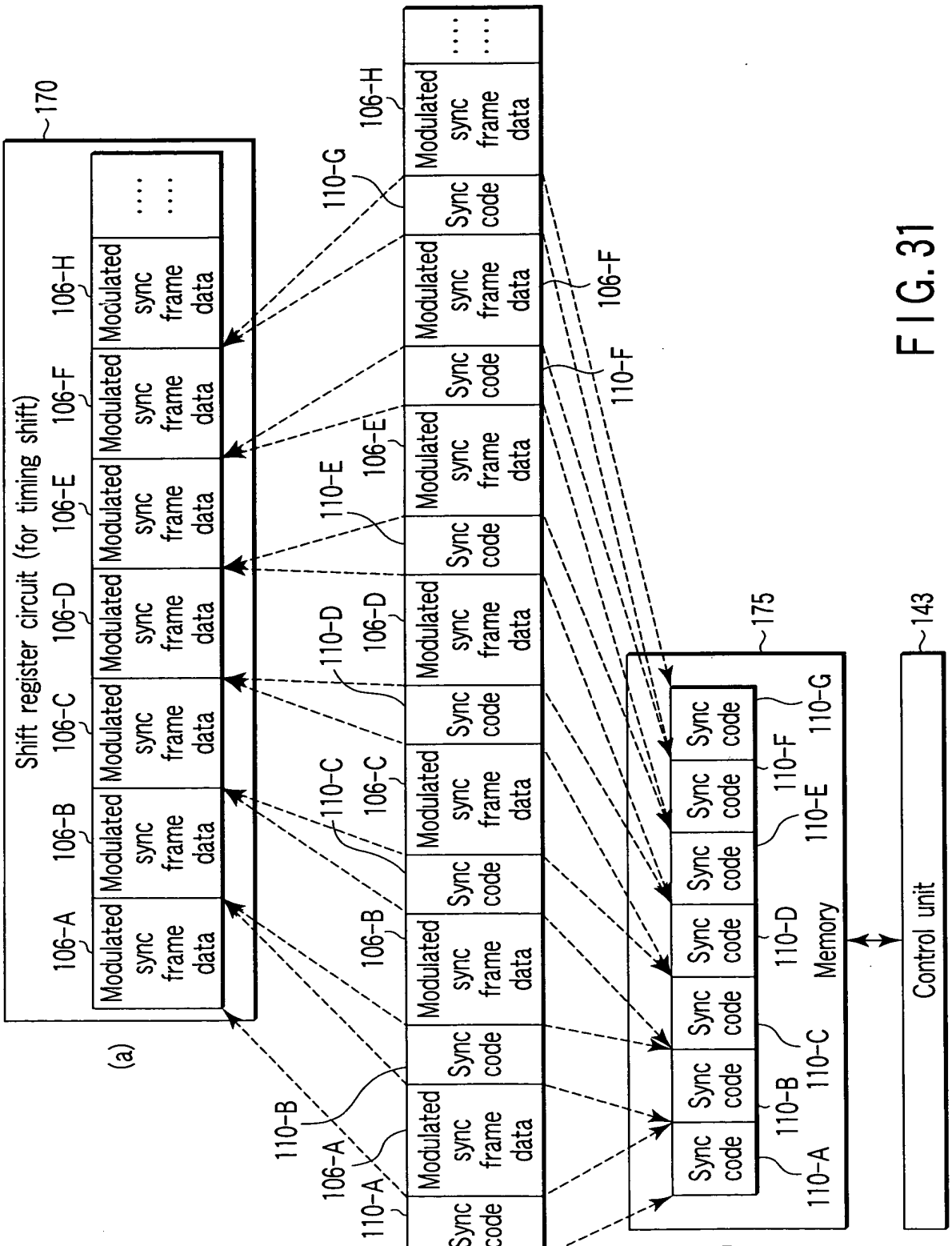

170
Shift register circuit (for timing shift)
106-A
106-B
106-C
106-D
106-E
106-F
106-H
Modulated sync frame data
(a)
110-G
110-F
110-E
110-D
110-C
110-B
110-A
Sync code
(b)
(c)
175
Memory
Control unit
143

FIG. 31

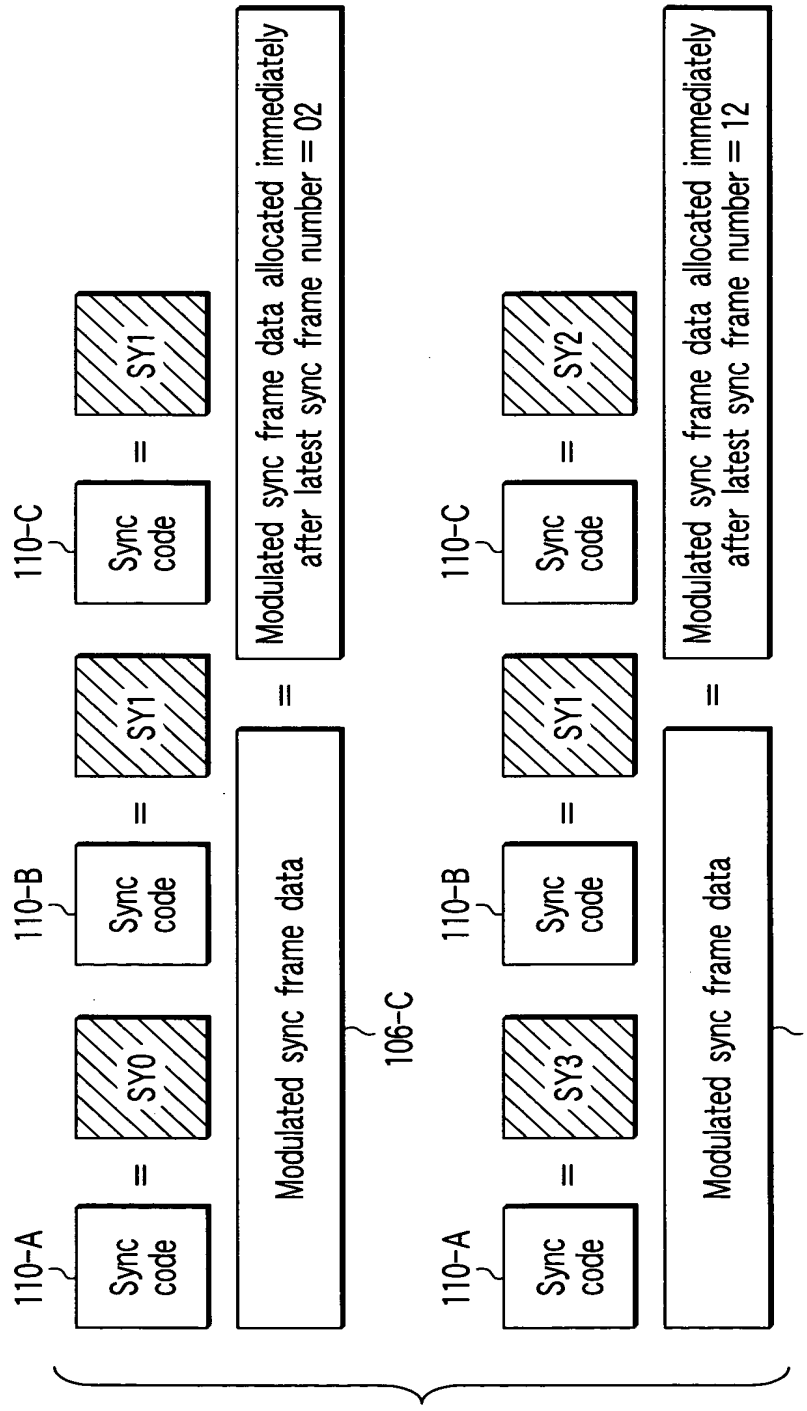

110-A
Sync code
=
SY0
110-B
Sync code
=
SY1
110-C
Sync code
=
SY1
Modulated sync frame data
106-C
=
Modulated sync frame data allocated immediately after latest sync frame number = 02
110-A
Sync code
=
SY3
110-B
Sync code
=
SY1
110-C
Sync code
=
SY2
Modulated sync frame data
106-C
=
Modulated sync frame data allocated immediately after latest sync frame number = 12

FIG. 32

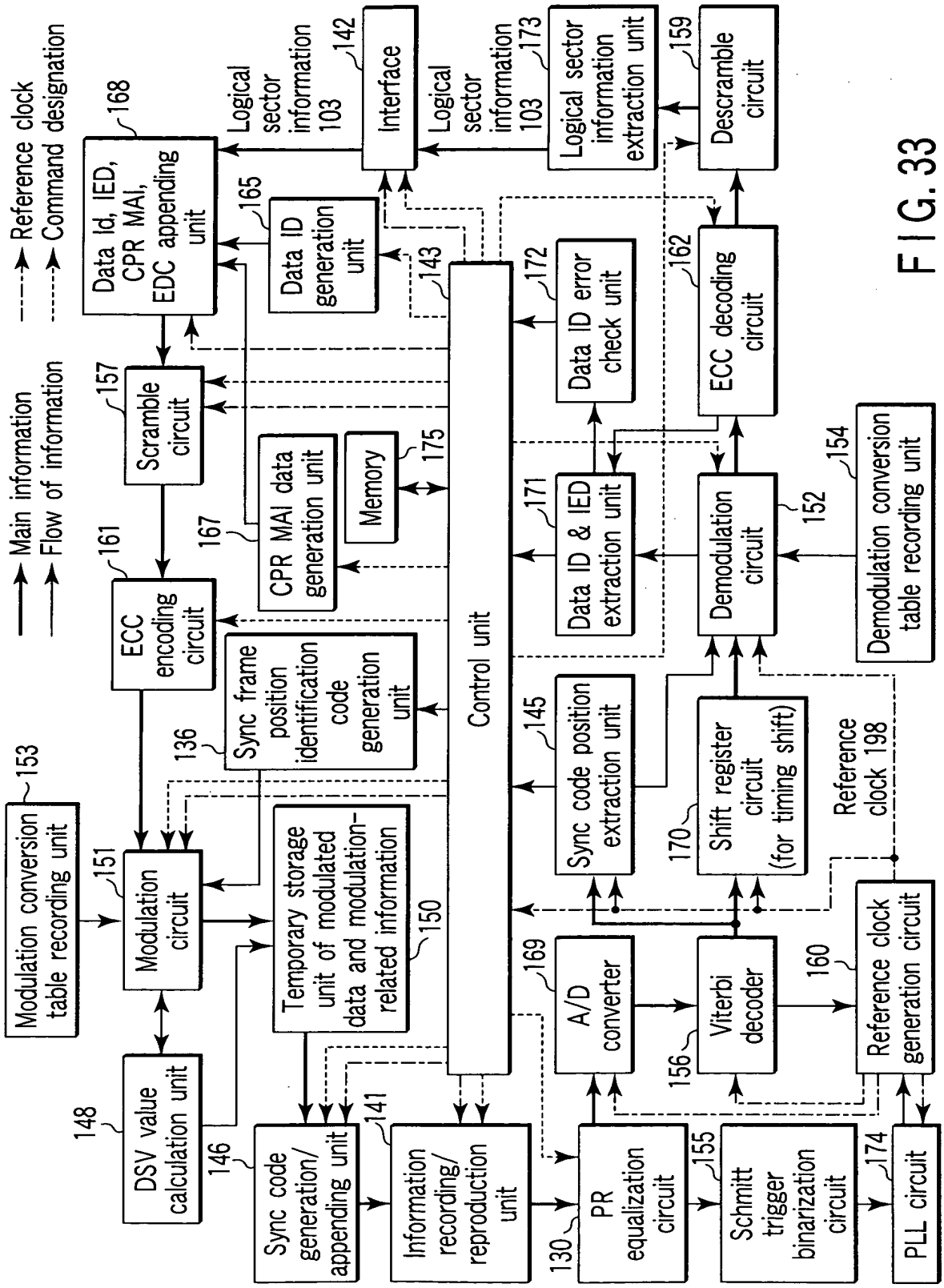

Main information
Flow of information
Reference clock
Command designation
Data Id, IED, CPR MAI, EDC appending unit
168
Logical sector information 103
Interface
142
Logical sector information 103
173
Logical sector information extraction unit
159
Descramble circuit
Data ID generation unit
165
143
Data ID error check unit
172
ECC decoding circuit
162
Scramble circuit
157
CPR MAI data generation unit
167
Memory
175
Control unit
Data ID & IED extraction unit
171
Demodulation circuit
152
154
Demodulation conversion table recording unit
ECC encoding circuit
161
Sync frame position identification code generation unit
136
Sync code position extraction unit
145
Shift register circuit (for timing shift)
170
Reference clock 198
Modulation conversion table recording unit
153
Modulation circuit
151
Temporary storage unit of modulated data and modulation-related information
150
A/D converter
169
Viterbi decoder
156
160
Reference clock generation circuit
DSV value calculation unit
148
Sync code generation/ appending unit
146
141
Information recording/ reproduction unit
PR equalization circuit
130
155
Schmitt trigger binarization circuit
174
PLL circuit

FIG. 33

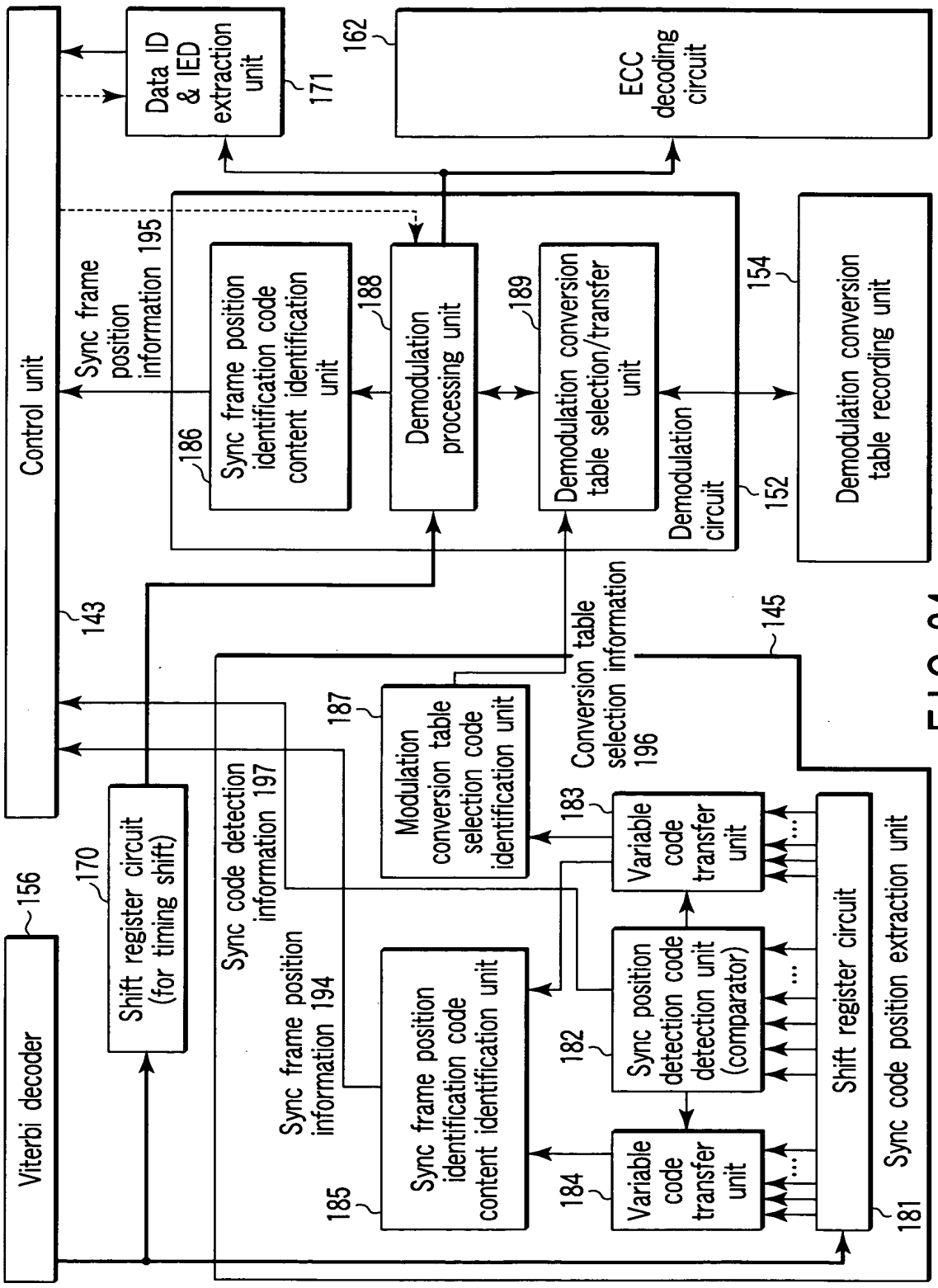

Control unit
Data ID & IED extraction unit
171
162
ECC decoding circuit
Sync frame position information 195
Sync frame position identification code content identification unit
186
188
Demodulation processing unit
189
Demodulation conversion table selection/transfer unit
Demodulation circuit
152
154
Demodulation conversion table recording unit
143
145
Conversion table selection information 196
Modulation conversion table selection code identification unit
187
183
Variable code transfer unit
Sync code detection information 197
Sync frame position information 194
Sync frame position identification code content identification unit
185
182
Sync position detection code detection unit (comparator)
184
Variable code transfer unit
Shift register circuit
181
Sync code position extraction unit
Viterbi decoder
156
170
Shift register circuit (for timing shift)

FIG. 34

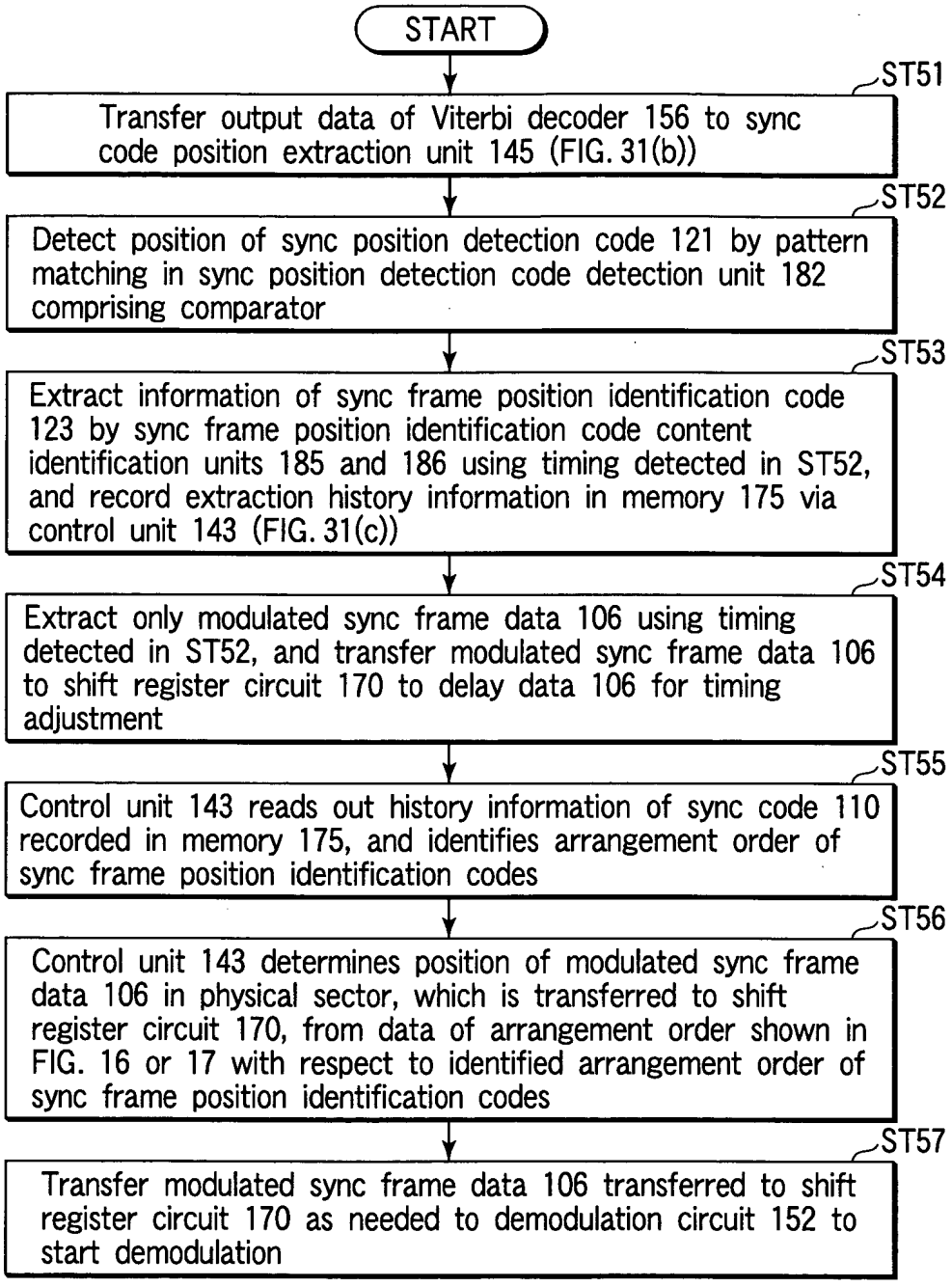

START
ST51
Transfer output data of Viterbi decoder 156 to sync code position extraction unit 145 (FIG. 31(b))
ST52
Detect position of sync position detection code 121 by pattern matching in sync position detection code detection unit 182 comprising comparator
ST53
Extract information of sync frame position identification code 123 by sync frame position identification code content identification units 185 and 186 using timing detected in ST52, and record extraction history information in memory 175 via control unit 143 (FIG. 31(c))
ST54
Extract only modulated sync frame data 106 using timing detected in ST52, and transfer modulated sync frame data 106 to shift register circuit 170 to delay data 106 for timing adjustment
ST55
Control unit 143 reads out history information of sync code 110 recorded in memory 175, and identifies arrangement order of sync frame position identification codes
ST56
Control unit 143 determines position of modulated sync frame data 106 in physical sector, which is transferred to shift register circuit 170, from data of arrangement order shown in FIG. 16 or 17 with respect to identified arrangement order of sync frame position identification codes
ST57
Transfer modulated sync frame data 106 transferred to shift register circuit 170 as needed to demodulation circuit 152 to start demodulation

FIG. 35

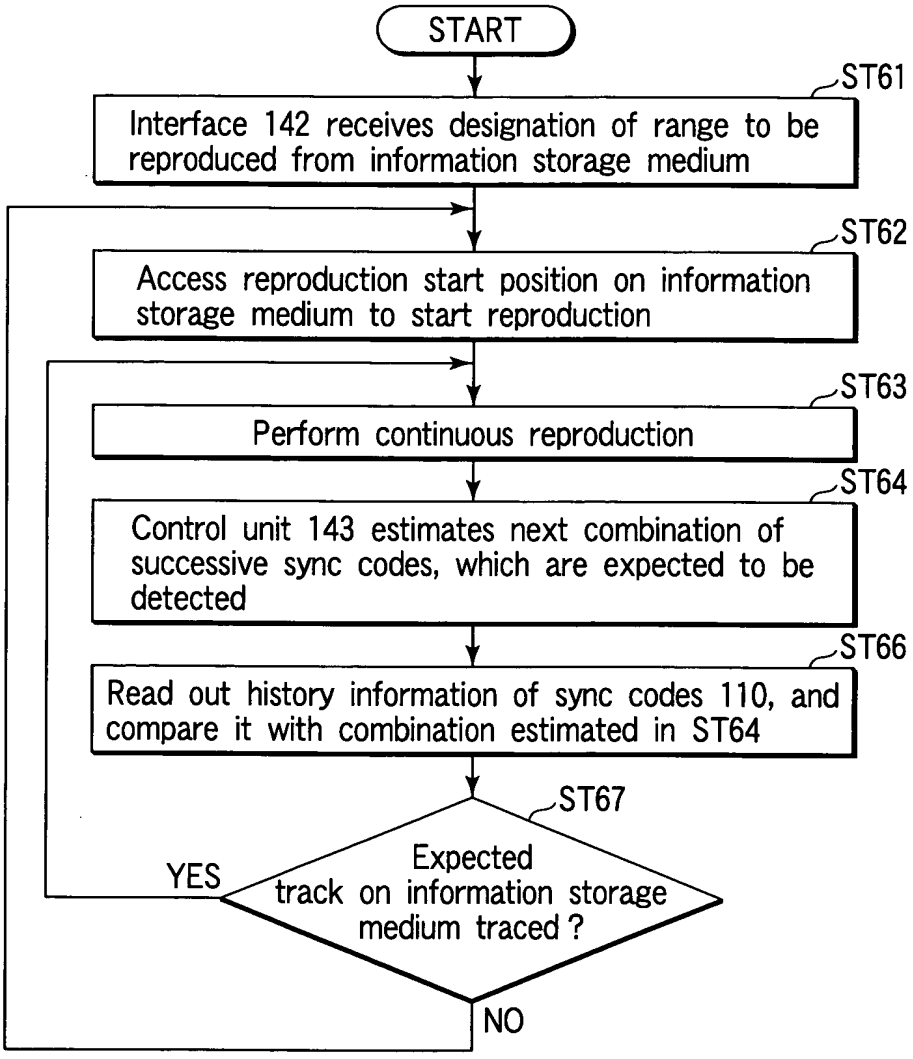

START
ST61
Interface 142 receives designation of range to be reproduced from information storage medium
ST62
Access reproduction start position on information storage medium to start reproduction
ST63
Perform continuous reproduction
ST64
Control unit 143 estimates next combination of successive sync codes, which are expected to be detected
ST66
Read out history information of sync codes 110, and compare it with combination estimated in ST64
ST67
Expected track on information storage medium traced ?
YES
NO

FIG. 36

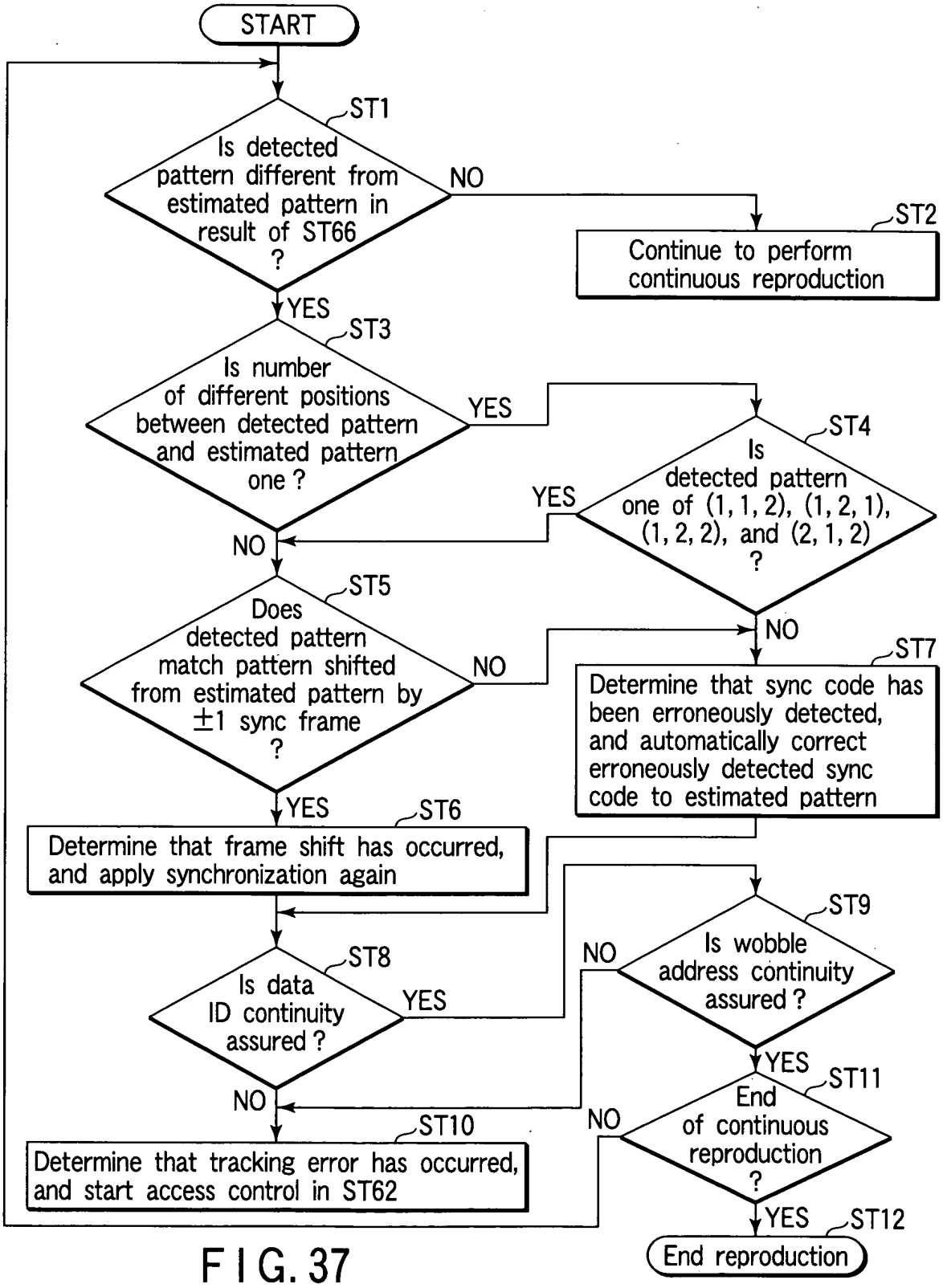

START
ST1
Is detected pattern different from estimated pattern in result of ST66 ?
NO
ST2
Continue to perform continuous reproduction
YES
ST3
Is number of different positions between detected pattern and estimated pattern one ?
YES
ST4
Is detected pattern one of (1, 1, 2), (1, 2, 1), (1, 2, 2), and (2, 1, 2) ?
YES
NO
ST5
Does detected pattern match pattern shifted from estimated pattern by ±1 sync frame ?
NO
NO
ST7
Determine that sync code has been erroneously detected, and automatically correct erroneously detected sync code to estimated pattern
YES
ST6
Determine that frame shift has occurred, and apply synchronization again
ST9
Is wobble address continuity assured ?
NO
ST8
Is data ID continuity assured ?
YES
YES
ST11
End of continuous reproduction ?
NO
NO
ST10
Determine that tracking error has occurred, and start access control in ST62
YES
ST12
End reproduction

FIG. 37

Combination effect number	⟨1⟩	⟨2⟩	⟨3⟩	⟨4⟩	⟨5⟩	⟨6⟩	⟨7⟩	⟨8⟩	⟨9⟩	⟨10⟩	⟨11⟩	⟨12⟩	⟨13⟩	⟨14⟩	⟨15⟩
A) File or folder separation between SD and HD	○		○		○		○		○		△	△	△	△	△
B) 4-bit expression of sub-picture information and compression rule		○		○		○		○		○	△	△	△	△	△
C) Allow to set a plurality of types of recording formats for read-only medium					○	○					○				
D) ECC block structure using product code					○	○	○	○	○	○					○
E) Distribute and allocate data in sectors to a plurality of small ECC blocks							○	○							○
F) Insert different PO group data for respective sectors									○	○					○
G) Segment division structure in ECC block			○	○	○	○	△	△	△	△	○	△	△	△	○
H) Guard area allocation structure between ECC blocks			△	△	○	○					○				
I) Guard areas are recorded to locally overlap each other											○				
J) Number of code changes upon shifting combination of sync codes ≧ 2	○	○					○	○	○	○					○
K) Set specific condition to address number assignment method													○		
L) L/G recording + wobble modulation	○	○	○	○										○	
M) Distribute and allocate unstable bits also on groove area												○		○	
N) Distribute and allocate unstable bits on land and groove												○			
O) ±90° wobble phase modulation															
P) Adopt gray codes or special track codes	○	○													

FIG. 38